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EXAMINER
CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/662,225	PLESSIER ET AL.	
	Examiner	Art Unit	
	MARDOCHEE CHERY	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is a reply to applicant's communication filed on April 22, 2008 in response to the Office action mailed on December 13, 2007, rejecting claims 1-10 and 12-20. Applicant's remarks and amendment to the claims were considered with the results that follow.

2. In response to the last Office action, claims 1, 8, 12, 14, and 15 are amended. Claims 1-10 and 12-20 remain pending.

3. The rejection of claim 12, under 35 U.S.C. 112, first paragraph is withdrawn in view of the remarks filed on April 22, 2008.

Response to Arguments

4. Applicant's arguments filed April 22, 2008 have been fully considered but they are not persuasive.

a. Applicant's representative, on page 9 of the remarks, points to section B of the Office action mailed on December 13, 2007 as purportedly supporting a direct contrast between the claimed invention and the operation of Iadanza (6,091,645). However, section B of that Office action is merely the Examiner's interpretation of the limitation argued by applicant with respect to claim 1, namely, "a data content of any memory element of the sub-array being rotatable

by shifts through the memory elements of the sub-array". There was no reference made to Iadanza in responding to applicant's arguments in section B of that Office action.

b. Applicant's representative further argues on page 9 of the remarks, that "each sub-array of Iadanza is not so isolated from the other sub-arrays".

Iadanza discloses "each memory sub-array is provided read/write coupling to respective first hierarchy signal lines of associated I/O data line hierarchy structures, and the first hierarchy signal lines of the respective hierarchy structures are isolated from one another and each memory sub-array may be interfaced in parallel or separately with respect to other memory sub-arrays; col. 22, lines 8-18; each memory sub-array may be selectively enabled independently of the other memory sub-arrays; col. 33, lines 5-10; the memory sub-arrays are to be operated as separate independent memory units; col. 33, lines 20-24".

Tomaiuolo discloses "the array is divided in two independent banks or semi-arrays, each having its own independent read path; and there are two totally independent and uncorrelated reading paths for the data stored in the two banks or semi-arrays of the memory device; two independent arrays of sense amplifiers of the two memory banks; pars. 0006, 0023, 0044".

c. Examiner is fully aware of applicant's remarks, on page 11, regarding the use of language such as "operable to" in some of the claims. While this language is perfectly permissible in patent claims, it only distinguishes over prior art structures that cannot or are not operable to perform the recited function. Indeed, the embodiments disclosed in Iadanza and Tomaiuolo are well "operable to allow random access and sequential", are also sufficiently "operable to cause the array to operate as a random access memory, and a first-in-first-out memory" claimed by applicant. No specific structure is required for such limitation. It suffices that a device posseses the capability to allow…, cause…, receive…, and shift… as claimed by applicant.

Specification

5. The disclosure is objected to because of the following informalities: while the title of the invention refers to a "bidimensional accessible memory", the claims, for instance independent claim 1, are directed to a "monodimensional accessible memory".

Appropriate correction is required.

Claim Objections

6. Claims 8-10 and 14-20 are objected to because of the following informalities:

d. In claim 8, line 2, it appears that "having a contents" should be changed to –having contents--.

e. In claim 8, line 3, it appears that "having a contents" should be changed to –having contents--.

f. Claims 8 and 14 recite "allow sequential access to the contents of the memory locations via a predetermined one of the memory locations during a second mode of operation, wherein the same predetermined one of the memory locations is used to allow sequential access to the contents of the memory locations". The second clause appear and render this limitation ambiguous for in the first clause it is clear that sequential access is already allowed to the predetermined one of the memory locations, and as stated, the second clause merely rephrase the first one. Such ambiguous could be fixed by replacing the occurrence of "sequential access" in the second clause with "random access" in which case support from the original disclosure is necessary.

g. The following limitations lack proper antecedent basis:

i. Claim 8, line 8, "the same predetermined".

ii. Claim 14, line 9, "the same predetermined one".

iii. Claim 15, line 4, "the contents"

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 8-10 and 12-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject

matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Particularly, claims 8, 12, 14, and 15 recite inter alias "...the same predetermined one of the memory locations is used to allow sequential access to the contents of the memory locations… or …allow access to a same predetermined one of the memory locations…". These limitations find no support in the original disclosure under 35 USC 112 first paragraph and consist new matter. See Waldemar Link, GmbH & Co. v. Osteonics Corp. 32 F.3d 556, 559, 31 USPQ2d 1855, 1857 (Fed. Cir. 1994); In re Rasmussen, 650 F.2d 1212, 211 USPQ 323 (CCPA 1981). See MPEP § 2163.06 - § 2163.07(b) for a discussion of the relationship of new matter to 35 U.S.C. 112, first paragraph.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 8-10 and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Tomaiuolo (2002/0087817).

As per claims 8 and 14-16, Tomaiuolo discloses a memory, comprising: a plurality of memory locations each having a contents [par. 006]; and a control circuit coupled to the memory locations and operable to, allow random access to the memory locations during a first mode of operation, and allow sequential access to the contents of the memory locations via a predetermined one of the memory locations during a second mode of operation [page 6, left column, par. 8], wherein the same predetermined one of the memory locations is used to allow sequential access to the contents of the memory locations [par. 0001, 0007-0009, 0011].

As per claim 9 Tomaiuolo discloses the first mode of operation comprises a read mode and the second mode of operation comprises a write mode [par. 004].

As per claim 10 Tomaiuolo discloses the first mode of operation comprises a write mode; and the second mode of operation comprises a read mode [par. 015].

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iadanza (6,091,645) in view of Applicant Admitted Prior Art (hereinafter APA).

As per claim 1, Iadanza discloses a memory comprising: at least one array of memory elements [col. 2, ll 28-35]; a partition of the at least one array into a plurality of sub-arrays of the memory elements [Fig. 1A-1D]; an array configuration circuit for selectively putting the at least one array in one of two operating configurations, the two operating configurations including [col. 2, ll 20-27]; a sub-array selector, responsive to a first memory address, for selecting one among the plurality of sub-arrays according to the first memory address, the sub-array selector enabling access to the selected sub-array [col. 2, ll 28-36]; and a memory element access circuit, responsive to a second memory address, for enabling access to a prescribed memory element in the selected sub-array after a prescribed number of shifts, depending on the second memory address, of the data content of the memory elements in the selected sub-array, the memory blocks of each sub-array being isolated from the memory blocks of the other sub-arrays [col. 22, lines 8-18, col. 33, lines 5-10, col. 33, lines 20-24], and a data content of any memory element of the sub-array being rotatable by shifts through the memory elements of the sub-array [col. 8, ll 36-50; col. 10, ll 29-42].

However, Iandaza does not specifically teach a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block as required by the claim.

APA discloses a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block [pars. 6 and 7] to provide a memory that can be accessed sequentially in a first-in, first-out manner and a memory that can be accessed randomly (pars. 6-7).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Iadanza to include a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block since this would have provided a memory that can be accessed sequentially in a first-in, first-out manner and a memory that can be accessed randomly (pars. 6-7) as taught by APA.

As per claim 2, Iadanza discloses said array configuration circuit includes, for each sub-array of memory elements, an input selector associated with a first memory element of the sub-array, for selectively feeding the first memory element with either an output of a last memory element in an adjacent previous sub-array, in the first operating configuration, or an output of a last memory element of the sub-array, in the second

operating configuration [col. 2, ll 52-65; col. 5, ll 66 to col. 6, ll 12].

As per claim 3, Iadanza discloses the first operating configuration is a data storage configuration, in which the memory is put when data are to be stored therein, and the second operating configuration is a data retrieval configuration, in which the memory is put when data are to be retrieved therefrom [col. 1, ll 62 to col. 2, ll 4; col. 2, ll 28-36].

As per claim 4, Iadanza discloses in the second operating configuration each sub-array provides a respective output data, the sub-array selector selecting one sub-array output data out of the plurality of output data provided by the plurality of sub-arrays, according to the first address [col. 2, ll 28-36].

As per claim 5, Iadanza discloses said memory element access circuit enables a transfer of the output data of the selected sub-array to a memory output after a prescribed number of shifts of the data content of the memory elements in the selected sub-array [col. 8, ll 36-50; col. 10, ll 29-42].

As per claim 6, Iadanza discloses said memory element access circuit includes a counter for counting the number of data content shifts, and a coincidence detector detecting coincidence between a counter value and a value representative of the second address, the coincidence detector enabling the transfer of the output data of the

selected sub-array to the memory output when the counter value equals the value representative of the second address [col. 2, ll 36-44; col. 10, ll 10-28; col. 35, ll 34-51; col. 33, ll 25-34].

As per claim 7, Iadanza discloses each memory element includes at least one flip-flop [col. 28, ll 42-52].

13. Claims 12-13 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomaiuolo (2002/0087817) in view of APA and further in view of Iadanza (6,091,645).

As per claim 12, Tomaiuolo discloses a memory, comprising: an array of memory locations [par. 005-006]; and a control circuit coupled to the array and operable to cause the array to operate as a random-access memory during a first mode of operation [page 6, left column, par. 8].

However, Tomaiuolo does not specifically teach a first-in-first-out memory during a second mode of operation as required by the claim.

APA discloses a first-in-first-out memory during a second mode of operation [Par. 006] to provide a memory that can be accessed sequentially in a first-in, first-out manner (pars. 6-7).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Tomaiuolo to include a first-in-first-out

memory during a second mode of operation since this would have provided a memory that can be accessed sequentially in a first-in, first-out manner (pars. 6-7) as taught by APA.

As per claim 12 Tomaiuolo further discloses the memory locations comprise rings of serially coupled memory locations each having a respective contents with the contents of each ring being independent of the contents of the other rings [page 6, left column, par. 8].

However, Tomaiuolo and APA do not specifically teach during the first mode of operation, the control circuit is operable to, receive a clock signal, shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal.

Iadanza discloses during the first mode of operation, the control circuit is operable to control each of the rings to, receive a clock signal, shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59] to provide serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Tomaiuolo and APA to include shifting

the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal since this would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

As per claim 13 Tomaiuolo discloses the memory locations comprise a ring of serially coupled memory locations each having a respective contents [page 6, left column, par. 8].

However, Tomaiuolo and APA do not specifically teach during the first mode of operation, the control circuit is operable to, receive a clock signal, shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal.

Iadanza discloses during the first mode of operation, the control circuit is operable to, receive a clock signal, shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59] to provide serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Tomaiuolo and APA to include shifting

the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal since this would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

As per claims 17-20, the rationale in the rejection of claim 12 is herein incorporated.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art

disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

16. When responding to the Office action, Applicant is advised to clearly point out where support, with reference to page, line numbers, and figures, is found for any amendment made to the claims.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S Sough/

Supervisory Patent Examiner, Art Unit 2188
07/24/08

July 23, 2008

Mardochee Chery
Examiner
AU: 2188